# LEAD FRAME WITH INTERDIGITATED PINS

## BACKGROUND

**[0001]** The present invention relates to packaging integrated circuits and pertains particularly to a lead frame with interdigitated pins.

**[0002]** In order to maximize lead frame density, pins for adjacent parts can be interdigitated. This is accomplished, for example, by designing packages so that the center position for pins is offset by one-half pitch distance on opposing sides of the package. This allows the pins of adjacent parts to be side-by side rather than end-to end. This provides sufficient room for interdigitating pins on the lead frames.

## SUMMARY OF THE INVENTION

**[0003]** In accordance with an embodiment of the present invention, a lead frame includes pins for a plurality of parts. The pins for the plurality of the parts include first pins for a first part and first pins for a second part. The first pins for the first part include first shaped pins and second shaped pins. Each of the first shaped pins has a wide area of a first length, and a narrow area. Each of the second shaped pins has a wide area of a second length and a narrow area. The first length and the second length are not equal. The first pins for the first part are interdigitated with the first pins for the second part.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0004]** Figure 1 shows a simplified top view of a portion of a lead frame in accordance with an embodiment of the present invention.

**[0005]** Figure 2 shows a simplified side view of a part with pins that provide varying amounts of inductance in accordance with an embodiment of the present invention.

**[0006]** Figure 3 shows a simplified side view of a part, with pins that provide varying amounts of inductance, attached to a printed circuit board in accordance with an embodiment of the present invention.

## DESCRIPTION OF THE EMBODIMENT

**[0007]** Figure 1 shows a simplified top view of a portion of a lead frame 10. Ground plate 11 is a ground plate for a first part. Ground plate 12 is a ground plate for a second part. For example lead frame 10 is composed of a base metal with precious metal plating.

**[0008]** The first part includes a pin 31, a pin 32, a pin 33, a pin 34, a pin 35, a pin 36, a pin 37, a pin 38, a pin 39, a pin 40, a pin 41, a pin 42, a pin 43, a pin 44, a pin 45, a pin 46, a pin 47, a pin 48, a pin 49 and a pin 50. As shown in Figure 1, pins 31 through 40 on a first side of the first part are offset from pins 41 through 50 on a second side of the first part. The offset allows for interleaving (interdigitating) of pins on adjacent parts.

**[0009]** The second part includes a pin 51, a pin 52, a pin 53, a pin 54, a pin 55, a pin 56, a pin 57, a pin 58, a pin 59, a pin 60, a pin 61, a pin 62, a pin 63, a pin 64, a

pin 65, a pin 66, a pin 67, a pin 68, a pin 69 and a pin 70. Only a portion of pin 61, pin 62, pin 63, pin 64, pin 65, pin 66, pin 67, pin 68, pin 69 and pin 70 are shown in Figure 1. As shown in Figure 1, pins 51 through 60 on a first side of the second part are offset from pins 61 through 70 on a second side of the second part. The offset allows for interdigitating of pins on adjacent parts.

**[0010]** Additionally, portions of two other parts are shown in Figure 1. For a third part, a pin 21, a pin 22, a pin 23, a pin 24, a pin 25, a pin 26, a pin 27, a pin 28, a pin 29 and a pin 30 are shown. For a fourth part, portions of a pin 71, a pin 72, a pin 73, a pin 74, a pin 75, a pin 76, a pin 77, a pin 78, a pin 79 and a pin 80 are shown.

**[0011]** For some critical paths, it is desired to reduce lead inductance. For these critical paths, the length of the wide area of each of the corresponding pins is increased. In order to still allow interdigitating, the length of the wide area of each of the surrounding pins of adjacent parts is correspondingly shortened.

**[0012]** For example, as shown in Figure 1, the length of the wide area of pin 41 of the first part has been increased. The lengths of the wide areas of surrounding pins 51 and 52 of the second part have been shortened. The length of the wide area of pin 42 of the first part has been increased. The lengths of the wide areas of surrounding pins 52 and 53 of the second part have been shortened. The length of the wide area of pin 45 of the first part has been increased. The lengths of the wide areas of surrounding pins 55 and 56 of the second part have been shortened. The length of the wide area of pin 46 of the first part has been

increased. The lengths of the wide areas of surrounding pins 56 and 57 of the second part have been shortened.

**[0013]** Likewise, the length of the wide area of pin 34 of the first part has been increased. The lengths of the wide areas of surrounding pins 23 and 24 of the third part have been shortened. The length of the wide area of pin 38 of the first part has been increased. The lengths of the wide areas of surrounding pins 37 and 38 of the third part have been shortened. The length of the wide area of pin 39 of the first part has been increased. The lengths of the wide areas of surrounding pins 38 and 39 of the third part have been shortened. The length of the wide area of pin 40 of the first part has been increased. The lengths of the wide areas of surrounding pins 29 and 30 of the third part have been shortened. And so on.

**[0014]** In Figure 1, the wide area for each pin is one of two distinct lengths; however, in alternate embodiments of the invention, there can be more than two different lengths for the wide areas of pins.

**[0015]** Figure 2 shows the first part having been assembled as an integrated circuit part 85. Pins 31 through 40 are shown. Because of the offset location, portions of pins 41 through 50 would normally be seen in a side view; however, for clarity in the drawing, pins 41 through 50 are not shown. A wide area 91 of pin 31 is, for example, approximately 1 millimeter (mm) wide and approximately 3.5 millimeters long. A narrow area 92 of pin 31 is, for example, approximately 0.5 mm wide and approximately 5.0 mm long. A wide area 93 of pin 40 is, for example, approximately 1 millimeter (mm) wide and

approximately 4.75 millimeters long. A narrow area 94 of pin 40 is, for example, approximately 0.5 mm wide and approximately 3.75 mm long.

**[0016]** Figure 3 shows integrated circuit part 85 attached to a printed circuit board (PCB) 86. Pins 31 through 40 are shown. Because of the offset locations, portions of pins 41 through 50 would normally be seen in a side view; however, for clarity in the drawing, pins 41 through 50 are not shown. As can be seen from Figure 3, all the pins of integrated circuit part 85 are inserted into PCB 86 and attached at the narrow areas. The wide areas of pins 31 through 50 do not come into physical contact with PCB 86.

**[0017]** The foregoing discussion discloses and describes merely exemplary methods and embodiments of the present invention. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Accordingly, the disclosure of the present invention is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.